



AMENDMENTS TO THE CLAIMS

2. (Currently amended) The A monolithic semiconductor device according to ~~claim 1~~ comprising:

a semiconductor substrate;

a plurality of microstructure stud capacitors formed over the substrate;

a brace transversely extending between lateral sides of at least two of the microstructure stud capacitors for supporting the at least two stud capacitors; and

a vertical space between said brace and said semiconductor substrate, wherein the brace comprises a dielectric material, and wherein the brace interconnects substantially all of the stud capacitors.

3. (Currently amended) The semiconductor device according to claim ~~[[1]]~~ 2, where the brace is located substantially near upper ends of the stud capacitors.

4. (Canceled)

5. (Currently amended) The semiconductor device according to claim ~~[[1]]~~ 2, wherein the brace comprises a microbridge structure extending above the substrate and between two or more of the stud capacitors.

6. (Currently amended) The semiconductor device according to claim [[1]] 2, where the stud capacitors each comprise a conductor material portion standing upright over the substrate, and wherein the brace interconnects the conductor material portions of two or more of the stud capacitors.

7. (Canceled)

8. (Currently amended) The semiconductor device according to claim [[1]] 2, wherein the stud capacitors each comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

9. (Currently amended) A monolithic semiconductor device comprising:

- a semiconductor substrate;
- a plurality of microstructure stud capacitors formed over the substrate;
- a brace transversely extending between lateral sides of at least two of the microstructure stud capacitors for supporting the at least two stud capacitors; and
- a vertical space between said brace and said semiconductor substrate~~[[;]]~~,

wherein the brace comprises a dielectric material.

10. (Previously presented) A monolithic semiconductor device comprising:

- a semiconductor substrate;

a plurality of microstructure stud capacitors formed over the substrate;

a brace transversely extending between lateral sides of at least two of the microstructure stud capacitors for supporting the at least two stud capacitors;

a vertical space between said brace and said semiconductor substrate; and

a dielectric layer between the substrate and the brace, where the brace is vertically spaced from the dielectric layer.

11. (Previously presented) A monolithic semiconductor device comprising:

a semiconductor substrate;

a plurality of microstructure stud capacitors formed over the substrate;

a brace transversely extending between lateral sides of at least two of the microstructure stud capacitors for supporting the at least two stud capacitors; and

a vertical space between said brace and said semiconductor substrate;

wherein the microstructure stud capacitors comprise conductive material and the brace comprises a dielectric.

12. - 22. (Canceled)

23. (Currently amended) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

a plurality of capacitor storage node microstructures formed over the substrate; and

a brace transversely extending between lateral sides of at least two of the microstructures for supporting the at least two of the microstructures, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure, wherein said brace comprises a dielectric material, and wherein there is a vertical space between said brace and said semiconductor substrate.

24. - 27. (Canceled)

28. (Currently amended) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

capacitor storage node microstructures formed over the substrate; ~~and~~

a brace transversely extending between lateral sides of at least two of the microstructures for supporting the at least two of the microstructures; and

a dielectric layer between said semiconductor substrate and said brace, wherein said brace is vertically spaced from said dielectric layer, ~~wherein~~ the microstructures comprise stud capacitors, and wherein there is a vertical space between said brace and said semiconductor substrate.

29. - 38. (Canceled)

39. (Previously Presented) A memory circuit, comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the microstructures, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure, and wherein there is a vertical space between said brace and said semiconductor substrate.

40. - 43. (Canceled)

44. (Previously Presented) A memory circuit, comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the microstructures, wherein the microstructures comprise stud capacitors, and wherein there is a vertical space between said brace and said semiconductor substrate.

45. - 76. (Canceled)

77. (Previously Presented) A processor system, comprising:

a processor; and

a memory circuit fabricated on a semiconductor chip communicating with the processor, said memory circuit comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the microstructures, wherein the capacitor microstructures comprise

capacitor studs, wherein there is a vertical space between said brace and said semiconductor substrate.

78. - 79. (Canceled)

80. (Currently amended) An in-process semiconductor device comprising:

a semiconductor substrate;

at least two microstructures formed over the substrate, said at least two microstructures comprising generally solid cylindrical shapes; ~~and~~

at least one brace transversely extending between lateral sides of said at least two microstructures, wherein said at least two microstructures are supported only by said at least one brace, and wherein said at least one brace comprises a single material layer; and

a dielectric layer between said semiconductor substrate and each of said at least one brace, where said at least one brace is vertically spaced from said dielectric layer.

81. (Currently amended) A semiconductor support structure, comprising:

a semiconductor substrate;

microstructures formed over the substrate; ~~and~~

a plurality of braces transversely extending between lateral sides of at least two of the microstructures for supporting the at least two of the microstructures, wherein the plurality of braces comprise a lattice support structure wherein said plurality of braces

intersect at said microstructures, and wherein there is a vertical space between said support structure and said semiconductor substrate; and

a dielectric layer between said semiconductor substrate and each of said plurality of braces, where said plurality of braces are vertically spaced from said dielectric layer.

82. - 83. (Canceled)

84. (Currently amended) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

a plurality of capacitor storage node microstructures formed over the substrate, said microstructures having vertical surfaces;

a brace transversely extending between the vertical surfaces of at least two of the microstructures for supporting the at least two of the microstructures, said brace being located substantially near the upper ends of said vertical surfaces of said microstructures; and

a vertical space between said brace and said substrate,

wherein the brace comprises a dielectric material.

85. (Currently amended) A semiconductor storage capacitor, comprising:

a semiconductor substrate;



capacitor storage node microstructures formed over the substrate, said microstructures having vertical surfaces; and

a plurality of braces transversely extending between the vertical surfaces of at least two of the microstructures for supporting the at least two of the microstructures, said plurality of braces being located substantially near the upper ends of said vertical surfaces of said microstructures, wherein said plurality of braces comprise a dielectric material, and wherein there is a vertical space between said plurality of braces and said semiconductor substrate.